Digital Power Monitor with Alert Output and Clear Pin

Preliminary Technical Data

ADM1192

FEATURES

Powered from 3.15 V to 26V
Precision Current Sense Amplifier
Precision Voltage Input
12-Bit ADC for Current and Voltage Readback
Alert output allow basic P-MOS hotswap up to 26V
SETV input for setting over current alert threshold
Programmable over-current filtering via TIMER pin
CLRB Input Pin
I²C Fast Mode compliant interface (400KHz max)
10-lead MSOP package

APPLICATIONS

Power Monitoring/Power Budgeting
Central office Equipment
Telecommunication and Data communication Equipment
PC/Servers

GENERAL DESCRIPTION

The ADM1192 is an integrated current sense amplifier that offers digital current and voltage monitoring via an on-chip 10-bit ADC, communicated through an I²C interface.

An internal current sense amplifier senses voltage across the sense resistor in the power path via the VCC and SENSE pins.

A 12-bit ADC is configured to be able to measure the current seen in the sense resistor, and also the supply voltage on the VCC pin.

An industry standard I²C interface allows a controller to read current and voltage data from the ADC. Measurements can be initiated by an I²C command. Alternatively the ADC can run continuously and the user can read the latest conversion data whenever it is required. Up to 4 unique I²C addresses can be created by the way the ADR pin is connected.

A SETV pin is also included. A voltage applied to this pin is internally compared to the output voltage on the current sense amplifier. When the output of SETV comparator asserts the current sense amplifier ouput exceeds the SETV voltage. This event is detected at the Alert block. The Alert block then charges up the external TIMER capacitor with a fixed current. When this timing cycle is complete the ALERT output asserts.

FUNCTIONAL BLOCK DIAGRAM

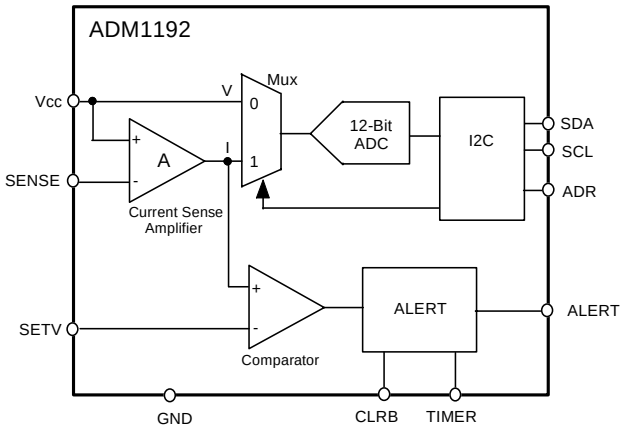

Figure 1.

APPLICATIONS DIAGRAM

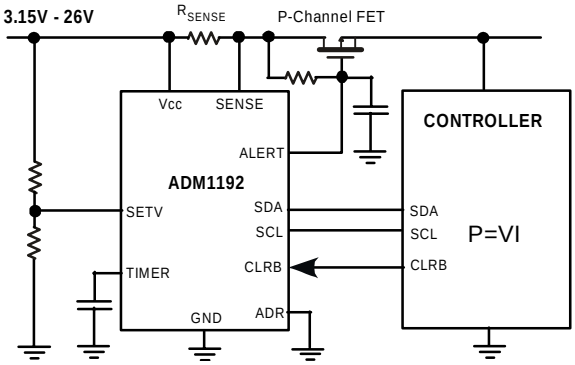

Figure 2.

A basic P-MOS hotswap circuit can be implemented with the Alert output. The value of the TIMER capacitor should be set so that the charging time of this capacitor is much longer than the period where a higher than nominal inrush current may be flowing.

The Alert output can also be used as a flag to warn a microcontroller or FPGA of an overcurrent condition. Alert outputs of multiple ADM1192 devices can be tied together and used as a combined alert.

The ADM1192 is packaged in a 10-lead MSOP package.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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REVISION HISTORY

05/06—Revision PrF: Initial Version

ADM1192—SPECIFICATIONS

V_{VCC} = 3.15V to 26V, T_A = -40°C to +85°C, Typical Values at T_A = +25°C unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Units	Conditions
VCC Pin					
Operating Voltage Range, V_{VCC}	3.15		26	V	
Supply Current, I_{CC}		1.6	3	mA	
Undervoltage Lockout, V_{UVLO}		2.8		V	V_{VCC} Rising
Undervoltage Lockout Hysteresis, $V_{UVLOHYST}$		25		mV	
CLRB Pin					
Low Input Voltage, $V_{CLRBLOW}$			0.8	V	
Pin Input Current for Logic 0 Input, $I_{CLRBLOW}$	-40	-22		µA	V_{CLRB} = 0V to 0.8V
High Input Voltage, $V_{CLRBHIGH}$	2			V	
Pin Input Current for Logic 1 Input, $I_{CLRBHIGH}$		3	10	µA	V_{CLRB} = 2.0V to 5.5V
Maximum Leakage Current, , $I_{CLRBLEAKMAX}$		TBD		µA	
ALERT Pin					
Output low voltage, $V_{ALERTOL}$		0.05	0.2	V	I_{ALERT} = -100µA
Maximum sink current, $I_{ALERTMAX}$	-2			mA	Maximum sink current allowed to flow in ALERT pin 0 output state
Input Current, I_{ALERT}	-1		1	µA	V_{ALERT} = V_{CC}; in Alert Condition
SENSE Pin					
Input Current I_{SENSE}	−1		+1	µA	V_{SENSE} = V_{VCC}
TIMER Pin					
Pull-Up Current (Overcurrent Fault), $I_{TIMERUPPMOC}$	-48	-60	-72	µA	(18.125 * V_{SENSE}) > V_{SETV}, V_{TIMER} = 1V
Pull-Down Current, $I_{TIMERDN}$		100		µA	Normal Operation, V_{TIMER} = 1V
Pin Threshold High, V_{TIMERH}	1.235	1.3	1.365	V	TIMER rising
SETV Pin					
Overcurrent Trip Threshold, $V_{SENSEOC}$	97.5	100	102.5	mV	V_{SETV} = 1.8125V; $V_{SENSEOC}$ = V_{VCC} - V_{SENSE}
Valid Input Range			1.9	V	
Input Current, $I_{SETVLEAK}$	-1		1	µA	V_{SETV} < 1.9V
		0.5		µA	V_{SETV} > 3.15V
ADR Pin					
Set address to 00, $V_{ADRLOWV}$	0		0.8	V	Low state
Set address to 01, $R_{ADRLOWZ}$	135	150	165	kΩ	Resistor to ground state, load pin with specified resistance for 01 decode
Set address to 10, $I_{ADRHIGHZ}$	−1		+1	µA	Open state, maximum load allowed on ADR pin for 10 decode
Set address to 11, $V_{ADRHIGHV}$	2		5.5	V	High state
Input current for 00 decode, I_{ADRLOW}		3	10	µA	V_{ADR} = 2.0 V to 5.5 V
Input current for 11 decode, $I_{ADRHIGH}$	−40	−22		µA	V_{ADR} = 0 V to 0.8 V
MONITORING ACCURACY[1]					
Current Sense Absolute Accuracy	TBD		TBD	%	V_{SENSE} = 75 mV
	−2.3		+2.2	%	V_{SENSE} = 75 mV, @ 0°C to +70°C
	TBD		TBD	%	V_{SENSE} = 50mV
	−2.5		+2.5	%	V_{SENSE} = 50 mV, @ 0°C to +70°C
	TBD		TBD	%	V_{SENSE} = 25mV
	−2.8		+2.8	%	V_{SENSE} = 25mV, @ 0°C to +70°C
	−3.5		+3.5	%	V_{SENSE} = 12.5 mV, @ 25°C
Current Sense Accuracy, T_C		±0.01		%/°C	
V_{SENSE} for ADC full-scale		105		mV	
Voltage Sense Accuracy	−1.5		+1.5	%	V_{VCC} = 3.15 V to 5.5V (VRANGE = 1)
	−1.5		+1.5	%	V_{VCC} = 10.8 V to 26V (VRANGE = 1)

Parameter	Min	Typ	Max	Units	Conditions
V_{CC} for ADC full-scale, low range		6.656		V	VRANGE = 1
V_{CC} for ADC full-scale, high range		26.628[2]		V	VRANGE = 0
I^2C Timing[3]					
Low level input voltage, V_{IL}			0.99	V	
High level input voltage, V_{IH}	2.31			V	
Low level output voltage on SDA, V_{OL}			0.4	V	I_{OL} = 3mA
Output fall time on SDA from V_{IHMIN} to V_{ILMAX}	20+0.1C_B		250	ns	C_B = bus capacitance from SDA to GND
Maximum width of spikes suppressed by input filtering on SDA and SCL pins	50		250	ns	
Input current, I_I, on SDA/SCL when not driving out a logic low	−10		+10	µA	
Input capacitance on SDA/SCL		5		pF	
SCL clock frequency, f_{SCL}			400	kHz	
LOW period of the SCL clock	600			ns	
HIGH period of the SCL clock	1300			ns	
Setup time for a repeated START condition, $t_{SU;STA}$	600			ns	
SDA output data hold time, $t_{HD;DAT}$	100			ns	
Set-up time for a stop condition, $t_{SU;STO}$	600			ns	
Bus free time between a STOP and a START condition, t_{BUF}	1300			ns	
Capacitive load for each bus line			400	pF	

[1] Monitoring accuracy is a measure of the error in a code that is read back for a particular voltage/current. This is a combination of amplifier error, reference error and ADC error.
[2]The maximum operating voltage is limited to V_{VCC} =13.2 V which corresponds to an ADC code of 508.
[3]The following conditions apply to all timing specifications: V_{BUS} =3.3V, T_A =25°C. All timings refer to V_{IHMIN} and V_{ILMAX}.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{CC} Pin	30 V
SENSE Pin	30 V
TIMER Pin	−0.3 V to +6 V
CLRB Pin	−0.3 V to +6 V
SETV Pin	30V
ALERT Pin	30 V
SDA, SCL Pins	−0.3 V to +6 V
ADR Pins	−0.3 V to +6 V
Power Dissipation	TBD
Storage Temperature	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability. Ambient temperature = 25°C, unless otherwise noted.

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

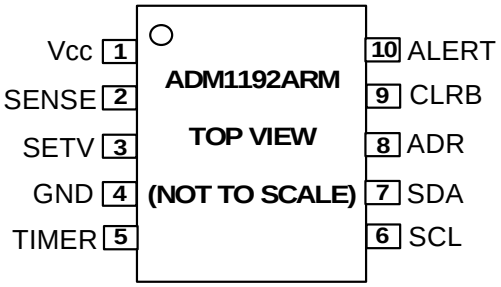

Figure 3. Pin Configurations

PIN FUNCTIONAL DESCRIPTIONS

Table 3.

Pin No.	Name	Description
1	VCC	Positive supply input pin. The operating supply voltage range is between 3.15 V to 26 V. An undervoltage lockout (UVLO) circuit resets the ADM1192 when a low supply voltage is detected.
2	SENSE	Current sense input pin. A sense resistor between the VCC and SENSE pins generates a voltage across a sense resistor. This voltage is proportional to the load current. A current sense amplifier amplifies this voltage before it is digitized by the ADC.
3	SETV	Input Pin. The voltage driven onto this pin will be compared to the output of the internal current sense amplifier. The lower the voltage on the SETV, the lower the current level that will cause a the ALERT output to assert.
4	GND	Chip Ground Pin
5	TIMER	Timer Input Pin. An external capacitor C_{TIMER} sets the timing period for masking overcurrent conditions. This timing period should be sufficient to allow the load charge up completely with maximum current at startup without tripping an overcurrent fault.
6	SCL	I^2C Clock Pin. Open-drain output requires an external resistive pull-up.
7	SDA	I^2C Data I/O Pin. Open-drain output requires an external resistive pull-up.
8	ADR	I^2C Address Pin. This pin can be tied low, tied high, left floating or tied low through a resistor to set four different I^2C addresses.
9	CLRB	Clear Pin. A latched overcurrent condition can be cleared by pulling this pin low.
10	ALERT	Alert Output Pin. Active high. This pin asserts when an overcurrent condition is present.

VOLTAGE AND CURRENT READBACK

The ADM1192 contains the components to allow voltage and current readback over an I²C bus. The voltage output of the current sense amplifier and the voltage on the VCC pin are fed into a 12-bit ADC via a multiplexer. The device can be instructed to convert voltage and/or current at any time during operation via an I²C command. When all conversions are complete the voltage and/or current values can be read out to 12-bit accuracy in two or three bytes.

SERIAL BUS INTERFACE

Control of the ADM1192 is carried out via the serial System Management Bus (I²C). This interface is compatible with fastmode I²C (400 kHz max). The ADM1192 is connected to this bus as a slave device, under the control of a master device.

GENERAL I²C TIMING

and show timing diagrams for general read and write operations using the I²C. The I²C specification defines specific conditions for different types of read and write operation, which are discussed later. The general I²C protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high to low transition on the serial data line SDA while the serial clock line SCL remains high. This indicates that a data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next 8 bits, consisting of a 7-bit slave address (MSB first) plus a R/W bit, which determines the direction of the data transfer, i.e. whether data will be written to or read from the slave device (0 = write, 1 = read).

   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit, and holding it low during the high period of this clock pulse. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/W bit is a 0, the master will write to the slave device. If the R/W bit is a 1, the master will read from the slave device.

IDENTIFYING THE ADM1192 ON THE I²C BUS

The ADM1192 has a 7-bit serial bus slave address. When the device is powered up, it will do so with a default serial bus address. The five MSBs of the address are set to 01011, the two LSBs are determined by the state of the ADR pin. There are four different configurations available on the ADR pin which correspond to four different I²C addresses for the two LSBs. These are explained in Table 4 below. This scheme allows four ADM1192 devices to operation on a single I²C.

Table 4. Setting I²C Addresses via the ADR Pin

ADR Configuration	Address
Low state	0x68
Resistor to GND	0x69
Floating (unconnected)	0x6A
High state	0x6B

2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an acknowledge bit from the slave device. Data transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low to high transition when the clock is high may be interpreted as a STOP signal.

   If the operation is a write operation, the first data byte after the slave address is a command byte. This tells the slave device what to expect next. It may be an instruction such as telling the slave device to expect a block write, or it may simply be a register address that tells the slave where subsequent data is to be written.

   Since data can flow in only one direction as defined by the R/W bit, it is not possible to send a command to a slave device during a read operation. Before doing a read operation, it may first be necessary to do a write operation to tell the slave what sort of read operation to expect and/or the address from which data is to be read.

3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will release the SDA line during the low period before the ninth clock pulse, but the slave device will not pull it low. This is known as No Acknowledge. The master will then take the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a STOP condition.

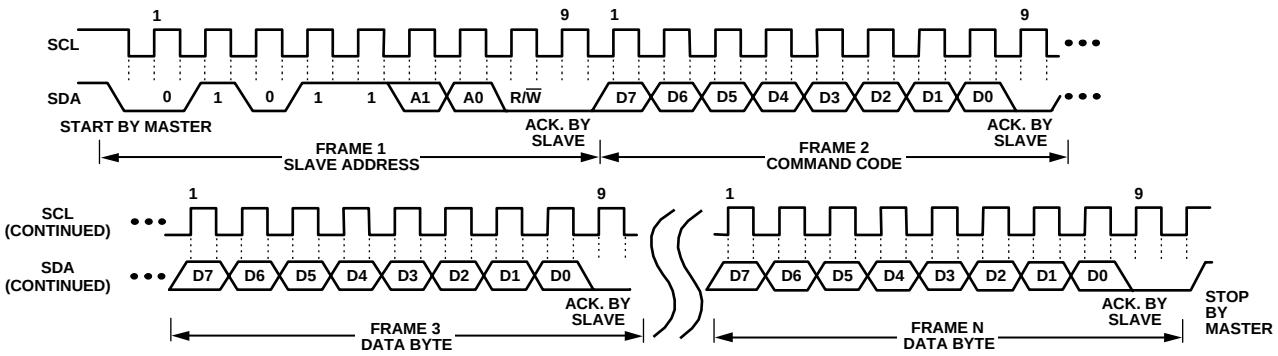

Figure 4. General I²C Write Timing Diagram

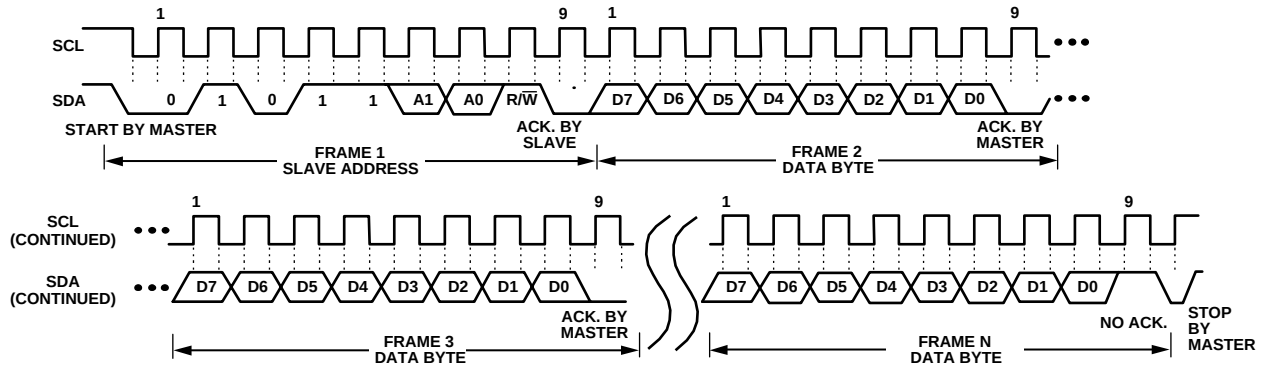

Figure 5. General I²C Read Timing Diagram

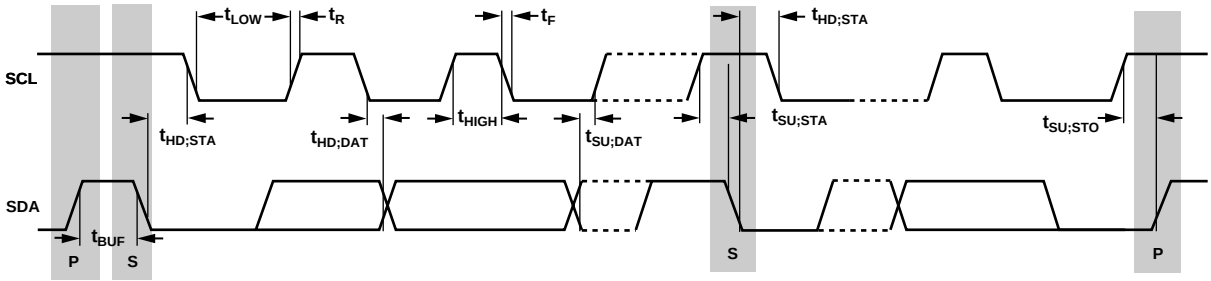

Figure 6. Serial Bus Timing Diagram

WRITE AND READ OPERATIONS

The I²C specification defines several protocols for different types of read and write operations. The ones used in the ADM1192 are discussed below. The following abbreviations are used in the diagrams:

Table 5. I²C abbreviations

S	START
P	STOP
R	READ
W	WRITE
A	ACKNOWLEDGE
N	NO ACKNOWLEDGE

QUICK COMMAND

This operation allows the master check if the slave is present on the bus. This entails the following:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.

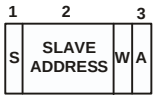

Figure 7. Quick Command

WRITE COMMAND BYTE

In this operation the master device sends a command byte to the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends the command byte. The command byte is identified by an MSB =0. (An MSB =1 indicates an Extended Register Write. See next section.)
5. The slave asserts ACK on SDA.
6. The master asserts a STOP condition on SDA to end the transaction.

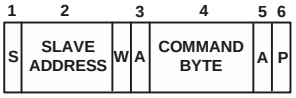

Figure 8. Command Byte Write

The seven LSBs of the command byte are used to configure and control the ADM1192. Details of the function of each bit are provided in .

Table 6. Command Byte Operations

Bit	Default	Name	Function
C0	0	V_CONT	Set to convert voltage continuously. If readback is attempted before the first conversion is complete, the ADM1192 will ACK and return all zeros in the returned data.
C1	0	V_ONCE	Set to convert voltage once. Self-clears. I²C will NACK an attempted read until ADC conversion is complete.
C2	0	I_CONT	Set to convert voltage continuously. If readback is attempted before the first conversion is complete, the ADM1192 will ACK and return all zeros in the returned data.
C3	0	I_ONCE	Set to convert current once. Self-clears. I²C will NACK an attempted read until ADC conversion is complete.
C4	0	VRANGE	Selects different internal attenuation resistor networks for voltage readback. A "0" in C4 selects a 14:1 voltage divider. A "1" in C4 selects a 7:2 voltage divider. With an ADC full-scale of 1.902 V, the voltage at the VCC pin for an ADC full-scale result is 26.63 V for VRANGE = 0 and 6.66 V for VRANGE = 1.
C5	0	N/A	Unused
C6	0	STATUS_RD	Status Read. When this bit is set the data byte read back from the ADM1192 will be the STATUS byte. This contains the status of the device alerts. See Table14 for full details of the status byte.

WRITE EXTENDED BYTE

In this operation the master device writes to one of the three extended registers of the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends the register address byte. The MSB of this byte is set to 1 to indicate an extended register write. The two LSBs indicate which of the three extended registers will be written to (see Table 7). All other bits should be set to 0.
5. The slave asserts ACK on SDA.
6. The master sends the command byte. The command byte is identified by an MSB = 0. (An MSB = 1 indicates an Extended Register Write. See next section.)
7. The slave asserts ACK on SDA.
8. The master asserts a STOP condition on SDA to end the transaction.

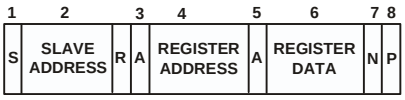

Figure 9. Command Byte Write

Table 8, Table 9, and give details of each extended register.

Table 7. Extended Register Addresses

A6	A5	A4	A3	A2	A1	A0	Extended Register
0	0	0	0	0	0	1	ALERT_EN
0	0	0	0	0	1	0	ALERT_TH
0	0	0	0	0	1	1	CONTROL

Table 8. ALERT_EN Register Operations

Bit	Default	Name	Function
0	0	EN_ADC_OC1	Enabled if a single ADC conversion on the I channel has exceeded the threshold set in the ALERT_TH register
1	0	EN_ADC_OC4	Enabled if four consecutive ADC conversions on the I channel have exceeded the threshold set in the ALERT_TH register
2	1	EN_OC_ALERT	Enables the OC_ALERT register. If an overcurrent condition is present and the TIMER pin has charged to 1.3V the OC_ALERT register will capture and latch this condition.
3	0	EN_OFF_ALERT	Enable an ALERT if the HS operation is turned off by an operation which writes the SWOFF bit high. This allows software override the Alert output (and will turn on a PMOS FET controlled by Alert).
4	0	CLEAR	Clears the OC_ALERT and ADC_ALERT status bits in the STATUS register. These may immediately reset if the source of the alert has not been cleared, or disabled with the other bits in this register. This bit self-clears to 0 after the STATUS register bits have been cleared.

Table 9. ALERT_TH Register Operations

Bit	Default	Function
7:0	FF	The ALERT_TH register sets the current level at which an alert will occur. Defaults to ADC full-scale. ALERT_TH 8-bit number corresponds to the top 8-bits of the current channel data.

Table 10. CONTROL Register Operations

Bit	Default	Name	Function
0	0	SWOFF	Force ALERT pin to de-assert. Can only be active if EN_OFF_ALERT bit is high (see Table 8).

READ VOLTAGE AND/OR CURRENT DATA BYTES

The ADM1192 can be set up to provide information in three different ways (see Write Command Byte section above). Depending on how the device is configured the following data can be read out of the device after a conversion (or conversions):

1. Voltage and Current Readback.

The ADM1192 will digitize both voltage and current. Three bytes will be read out of the device in the following format:

Table 111.

Byte	Contents	B7	B6	B5	B4	B3	B2	B1	B0
1	Voltage MSBs	V11	V10	V9	V8	V7	V6	V5	V4
2	Current MSBs	I11	I10	I9	I8	I7	I6	I5	I4
3	LSBs	V3	V2	V1	V0	I3	I2	I1	I0

2. Voltage Readback.

The ADM1192 will digitize voltage only. Two bytes will be read out of the device in the following format:

Table 12.

Byte	Contents	B7	B6	B5	B4	B3	B2	B1	B0
1	Voltage MSBs	V11	V10	V9	V8	V7	V6	V5	V4
2	Voltage LSBs	V3	V2	V1	V0	0	0	0	0

3. Current Readback.

The ADM1192 will digitize current only. Two bytes will be read out of the device in the following format:

Table 13.

Byte	Contents	B7	B6	B5	B4	B3	B2	B1	B0
1	Current MSBs	I11	I10	I9	I8	I7	I6	I5	I4
2	Current LSBs	I3	I2	I1	I0	0	0	0	0

The following series of events occur when the master receives three bytes (voltage and current data) from the slave device:

1. The master device asserts a START condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives the first data byte.
5. The master asserts ACK on SDA.
6. The master receives the second data byte.
7. The master asserts ACK on SDA.
8. The master receives the third data byte.
9. The master asserts NO ACK on SDA.
10. The master asserts a STOP condition on SDA and the transaction ends.

For the cases where the master is reading voltage only or current only, only two data bytes will be read and events 7 and 8 above will not be required.

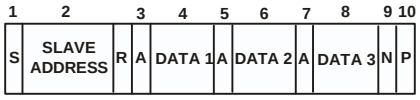

Figure 10. Three Byte Read fromADM1191

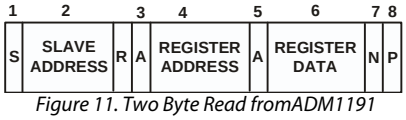

Figure 11. Two Byte Read fromADM1191

Read Status Register

A single register of status data can also be read from the ADM1192.

1. The master device asserts a START condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives the status byte.
5. The master asserts ACK on SDA.

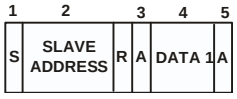

Figure 12. Status Read fromADM1191

Table 14 shows the ADM1192 status registers in detail. Note that bits 1, 3 and 5 are cleared by writing to bit 4 of the ALERT_EN register (CLEAR).

Table 14. Status Byte Operations

Bit	Name	Function
0	ADC_OC	An ADC based overcurrent comparison has been detected on the last 3 conversions
1	ADC_ALERT	An ADC based overcurrent trip has happened, which has caused the ALERT. Cleared by writing to bit 4 of the ALERT_EN register.
2	OC	An overcurrent condition is present (i.e. the output of the current sense amplifier is greater than the voltage on the SETV input).
3	OC_ALERT	An overcurrent condition has caused the Alert block to latch a fault on the ALERTB output has asserted. Cleared by writing to bit 4 of the ALERT_EN register.
4	OFF_STATUS	Set to 1 by writing to the SWOFF bit of the CONTROL register.
5	OFF_ALERT	An alert has been caused either by the SWOFF bit. Cleared by writing to bit 4 of the ALERT_EN register.

ALERT OUTPUT

The Alert output is an open-drain pin with 30V tolerance. There are two uses for this output:

1. **Overcurrent flag:**
   The Alert pin can be connected to an general purpose logic input of a controller. Under normal operation the ADM1192 will drive this output low. When an overcurrent condition occurs the output will assert high. An external pull-up resistor should be used.

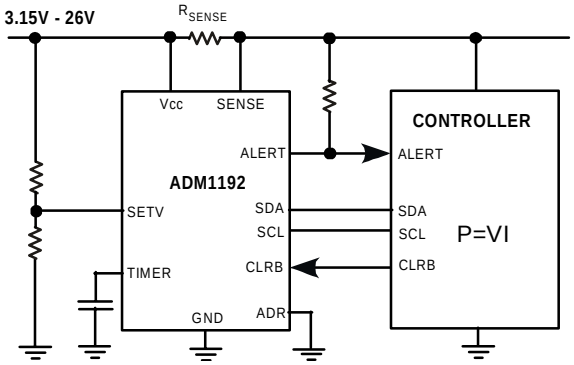

Figure 13. Using the ALERTB output as an interrupt

2. **Implementing a basic hotswap circuit:**
   A basic P-MOS hotswap circuit can be created. The Alert output should be connected to the GATE pin of a P-MOS FET connected in series with the power path. A pull-up from GATE to source will ensure that the PMOS GATE will be pulled up and the device held off as soon as power is applied. When the ADM1192 powers up the GATE will be pulled low by the Alert output. A capacitor on the will determine the slew rate of the GATE at turn-on. Note that if a current fault occurs at any point in operation the Alert output will assert high, turning off the P-MOS FET.

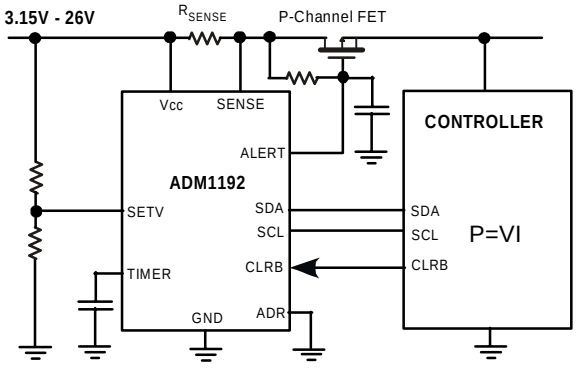

Figure 14. PMOS hotswap implemenation

SETV PIN

The SETV pin allows the user adjust the current level that trips the ALERT output. The output of the current sense amplifier is compared with the voltage driven onto the SETV pin. If the current sense amplifier output is higher than the SETV voltage then the output of the comparator will assert. By driving a different voltage onto the SETV pin the ADM1192 will detect an overcurrent condition at a different current level.

When the output of the SETV comparator asserts this tells the ALERT block to begin charging the external TIMER capacitor with a 60uA charging current. When the voltage on the TIMER capacitor reaches 1.3V the charging cycle is complete. The ALERT output will then assert (go high). Different values of TIMER capacitor will generate different time delays between current faults occurring and the ALERT output asserting. When using the ALERT output to implement a hotswap circuit the TIMER capacitor should be chosen to generate a large enough startup delay to allow the maximum inrush current completely charge up the load without tripping an ALERT fault.

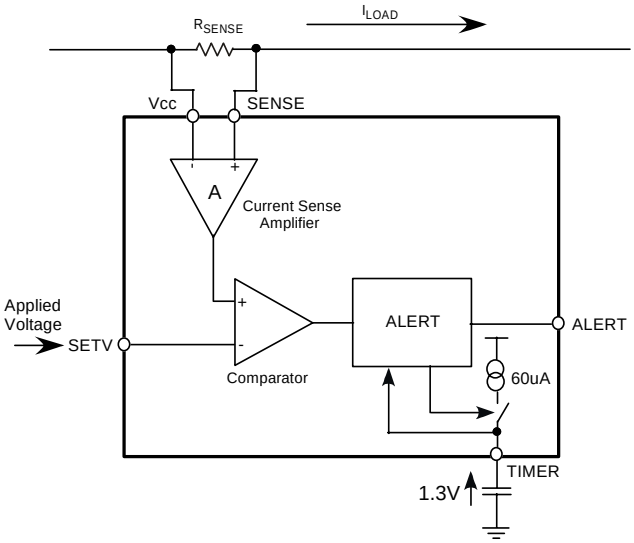

Figure 15 . SETV operation

KELVIN SENSE RESISTOR CONNECTION

When using a low-value sense resistor for high current measurement the problem of parasitic series resistance can arise. The lead resistance can be a substantial fraction of the rated resistance making the total resistance a function of lead length. This problem can be avoided by using a Kelvin sense connection. This type of connection separates the current path through the resistor and the voltage drop across the resistor. Figure 16 below shows the correct way to connect the sense resistor between the VCC and SENSE pins of the ADM1192.

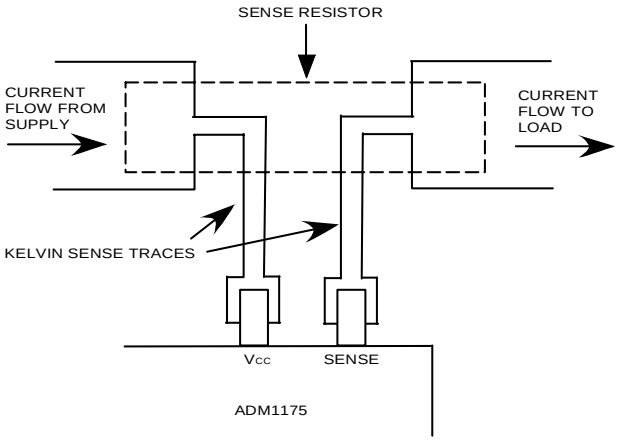

Figure 16. Kelvin Sense Connections

OUTLINE DIMENSIONS

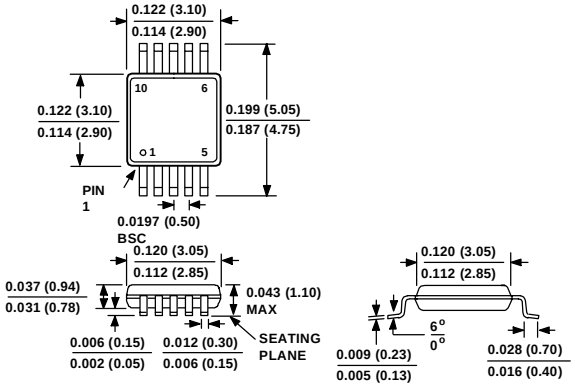

Figure 13. 10-Lead MSOP Package
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Brand	Temperature Range	Package Description	Package Outline
ADM1192-1ARMZ-R7[1]	M5M	-40°C to +85°C	MSOP-10	RM-10

[1] Z=PB-free part